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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,575	07/22/2003	Koichi Sato	NEG-299 US	6547

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EXAMINER
ROSSOSHEK, YELENA

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,575	SATO ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~01/04/2006~~. 10/28/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/623,575 filed 07/22/2003 and amendment filed 10/28/2005.

2. Claims 1-19 are pending in the Application. Claims 13-19 have been added to the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Objections

4. Claims 2, 3,4, 5, 6, 9, 10, 11, 12, 19 are objected to because of the following informalities: these claims have copulative "and/or", which has to be modified. In order to have definite claim language, Applicants have to choose either "and" or "or".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2, 4, 8, 10, 14 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the use of the term "discriminating" is vague, where it is not clear what relationship between the term "discriminating" and "type of the storage element". Moreover it is not definite what Applicant intent to mean by term "type of the storage element"; is it type of register (Reg1, Reg2 . . .), or type of register (gate, flip-flop), or

type of memory (register or other type of memory)? And, finally, there is a gap in relationship between terms "discriminating", "type of the storage element" and "in regard to an array-variable part", wherein it's unclear what is it "type of the storage element"? The Specification support these terms, but does not give straight forward explanation, for example, pages 10-14.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikegami (US Patent 6,782,354).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 1 and 7 Ikegami teaches an apparatus and method for estimating power consumption within the method and system (col. 2, ll.44-45; col. 3,

ll.11-14; col. 9, l.26), comprising: an behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information within model converting tool 13 having a tool of the behavior synthesis tool 12 as shown on the Fig. 2 for converting algorithm description 3 into the clock level model 8 (col. 6, ll.15-18) including GUI controller 41 shown on the Fig. 4 to obtain the correspondence relationships between plurality of registers 34 and plurality of memories 35 (col. 7, ll.40-48) wherein the data is behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 shown on the Figs. 3 and 4 (col. 7, ll.49-57); and a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information within clock base simulator 14 shown on the Fig. 2, which obtains the data from the clock level model 8 including the data as behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 (col. 6, ll.63-67; Figs. 3 and 4), wherein during the clock level verification process (col. 8, l.37) the precise estimation of power consumption is performed (col. 9, l.24).

With respect to claims 13 Ikegami teaches a method of simulation of a device within the method (col. 2, ll.44-45), comprising: providing, into a clock-based simulation module, a clock-based description and behavioral synthesis information, the behavioral synthesis information including information for describing which of alternative types of

storage units are to be simulated within model converting tool 13 having a tool of the behavior synthesis tool 12 as shown on the Fig. 2 for converting algorithm description 3 into the clock level model 8 (col. 6, ll.15-18) including GUI controller 41 shown on the Fig. 4 to obtain the correspondence relationships between plurality of registers 34 and plurality of memories 35 (col. 7, ll.40-48) wherein the data is behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 shown on the Figs. 3 and 4 (col. 7, ll.49-57), wherein clock base simulator 14 shown on the Fig. 2, obtains the data from the clock level model 8 including the data as behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 (col. 6, ll.63-67; Figs. 3 and 4), wherein during the clock level verification process (col. 8, l.37) the precise estimation of power consumption is performed (col. 9, l.24); and executing a clock-based simulation in the clock-based simulation module within clock-based simulator 14 shown on the Fig. 2 for carrying out (executing) a click level simulation based on the clock level simulation model 8 (col. 6, ll.21-23).

With respect to claims 2-6, 8-12 and 14 Ikegami teaches:

Claims 2, 8 and 14: the power consumption factor of the storage element is calculated by discriminating the type of the storage element using the behavioral synthesis information in regard to an array-variable part since the data variable/register/status (behavioral synthesis information) is input for the clock verification process including the power consumption performance (col. 9, l.24), wherein the data variable/register/status is generated by algorithm description 3 shown on the

Fig. 2 and stored in the tables 23 and 24 (col. 6, ll.63-67; Figs. 3 and 4), wherein this data is represented as sets of variables shown on the Figs. 5, 6, 9 and 10 (col. 9, ll.37-45, 49-51);

Claims 3 and 9: the power consumption factor is toggle rate and/or transition probability within scheduling the functions, obtained from algorithm description 3 (Fig. 2), and based on clocks in units of groups of allowable status transitions of variables related to the algorithm description model (col. 2, ll.55-63);

Claims 4 and 10: the power consumption factor is toggle rate and/or transition probability within controllers 36 and calculation operation transition 38 shown on the Fig. 4, wherein finite state machine (FSM) 21 shown on the Fig. 3 controlling state transitions of plurality of registers resources and memories resources (col. 7, ll.40-48; col. 6, ll.59-62; col.7, ll.32-37);

Claims 5 and 11: correspondence between RT variable names and gates is assumed from the behavioral synthesis information, and toggle rates and/or transition probabilities are set in gate circuits, thereafter the toggle rates and/or transition probabilities of all gate circuits being calculated within the data variable/register/status is generated by algorithm description 3 shown on the Fig. 2 and wherein the data is behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 shown on the Figs. 3 and 4 (col. 7, ll.49-57) within the capability of the technique to switch between the simulation in a gate level model and the simulation in an electronic circuit (register, memory) level model (col. 2, ll.5-7);

Claims 6 and 12: a gated clock is provided, the toggle rate and/or transition probability of a clock are made the same as the write probability with respect to a storage element since the terminals of the gates circuit correspond to the terminals of the electronic circuits (col. 2, ll.8-9).

With respect to claims 15-19 Ikegami teaches:

Claim 15: the clock-based description is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by the behavioral synthesizing unit within model converting tool 13 having a tool of the behavior synthesis tool 12 as shown on the Fig. 2 for converting algorithm description 3 into the clock level model 8 (col. 6, ll.15-18) including GUI controller 41 shown on the Fig. 4 to obtain the correspondence relationships between plurality of registers 34 and plurality of memories 35 (col. 7, ll.40-48);

Claim 16: the information on storage unit type is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by the behavioral synthesizing unit within model converting tool 13 having a tool of the behavior synthesis tool 12 as shown on the Fig. 2 for converting algorithm description 3 into the clock level model 8 (col. 6, ll.15-18) including GUI controller 41 shown on the Fig. 4 to obtain the correspondence relationships between plurality of registers 34 and plurality of memories 35 (col. 7, ll.40-48) wherein the data is behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 shown on the Figs. 3 and 4 (col. 7, ll.49-57);

Claim 17: the power consumption factor comprises at least one of a toggle rate and a transition probability within controllers 36 and calculation operation transition 38 shown on the Fig. 4, wherein finite state machine (FSM) 21 shown on the Fig. 3 controlling state transitions of plurality of registers resources and memories resources (col. 7, ll.40-48; col. 6, ll.59-62; col.7, ll.32-37);

Claim 18: assuming a correspondence between RT variable names and gates from the behavioral synthesis information; setting at least one of toggle rates and transition probabilities in gate circuits; and calculating toggle rates and transition probabilities of all gate circuits within the data variable/register/status is generated by algorithm description 3 shown on the Fig. 2 and wherein the data is behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 shown on the Figs. 3 and 4 (col. 7, ll.49-57) within the capability of the technique to switch between the simulation in a gate level model and the simulation in an electronic circuit (register, memory) level model (col. 2, ll.5-7);

Claim 19: if a gated clock is provided, the toggle rated and/or transition probability of a clock are made the same as write probability with respect to a storage element since the terminals of the gates circuit correspond to the terminals of the electronic circuits (col. 2, ll.8-9).

Remarks

9. In the remarks Applicants argue in substance:

a) there is no teaching or suggestion in Ikegami that the memory units be anything other than registers.

b) Hence, turning to the clear language of the claims, in Ikegami there is no teaching or suggestion of: "...a behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information; and a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information."

c) the locations in Ikegami to which the Examiner points do not provide any indication that different types of alternative storage elements are available for simulation by the clock-based simulation

d) the clock simulation of Ikegami is not all described as corresponding to a technique that uses "toggle rate" or "transition probability"

10. Examiner respectfully disagrees for the following reasons:

As to a) In response to applicant's argument that Ikegami fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "memory units be anything other than registers") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Moreover Ikegami teaches that simulation model 31

shown on the Fig. 4 is composed of a module I/O section 32, wherein the model I/O section 32 has an I/O register structure and an I/O memory structure (col. 7, ll.15-23).

As to b) as shown on the Fig. 2 Ikegami teaches a clock-level verification system 6 which contains model converting tool 13 comprising **behavioral synthesis information obtained from behavioral synthesis tool 12**, and clock level simulation (SIM) model 8 described by a clock level description (col. 6, ll.10-12, 16-19), wherein the information from both 12 and 8 is obtained by the clock base simulator 14 which executes the clock level simulation (col. 6, ll.21-24).

As to c) Ikegami teaches that simulation model 31 shown on the Fig. 4 is composed of a module I/O section 32, wherein the model I/O section 32 has an I/O register structure and an I/O memory structure (col. 7, ll.15-23).

As to d) Ikegami teaches scheduling the functions, obtained from algorithm description 3 (Fig. 2), and based on clocks in units of groups of allowable status transitions of variables related to the algorithm description model (col. 2, ll.55-63), wherein the clock base simulator 14, shown on the Fig. 2, obtains the data from the clock level model 8 including the data as behavioral synthesis information such as a register value R and status position value S stored in the tables 23 and 24 (col. 6, ll.63-67; Figs. 3 and 4), wherein during the clock level verification process (col. 8, l.37) the precise estimation of power consumption is performed (col. 9, l.24).

Based on at least these disclosures in Ikegami the rejection under 35 USC § 102 is maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center Z800